

SYNCHRONOUS DRAM UTILIZABLE AS SHARED MEMORY

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ABSTRACT OF THE DISCLOSURE

A memory array is divided into a plurality of blocks. A plurality of mode storage units is so disposed as to correspond to the memory blocks. When a plurality of controllers outputs a mode setting instruction at the time of making of power, a setting unit 113 sets control information designated by the mode setting instruction to the corresponding mode storage unit. When different controllers gain access to a synchronous DRAM, an access operation is executed for the corresponding memory block in accordance with the control information.

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